Amendments to the Claims

This listing of claims supersedes any previous submissions.

1. (Currently Amended) A method of manufacturing a trench-gate silicon semiconductor device (4), the method including forming trenches (20) in a semiconductor body (40) in an active transistor cell area of the device, the trenches (20) each having a trench bottom and trench sidewalls, and providing silicon oxide gate insulation (21A, 21B) in the trenches such that the gate insulation (21B, 33) at the trench bottoms is thicker than the gate insulation (21A, 24) at the trench sidewalls, wherein the method includes, after forming the trenches (20), the steps of:

forming a silicon oxide layer (24) at the trench bottoms and trench sidewalls; depositing a layer of doped polysilicon (34) adjacent the trench bottoms and trench side walls;

forming silicon nitride spacers (32) on the doped polysilicon (21) adjacent the trench sidewalls leaving the doped polysilicon exposed at the trench bottoms; thermally oxidising the exposed doped polysilicon to grow said thicker gate insulation (33) at the trench bottoms;

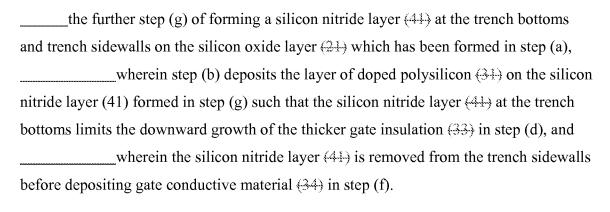
removing the silicon nitride spacers (32); and providing gate conductive material (34) within the trenches.

- 2. (Currently Amended) A method as claimed in claim 1, The method as recited in claim

 1.

 wherein step (b) deposits the layer of doped polysilicon (34) on the silicon oxide layer (24) formed in step (a), and

 wherein step (d) grows the thicker gate insulation (33) below the nitride spacers (32).
- 3. (Currently Amended) A method as claimed in claim 1, The method as recited in claim 1, including



- 4. (Currently Amended) A method as claimed in any one of claims 1 to 3, The method as recited in claim 1,
- wherein the silicon oxide layer (21) formed at the trench sidewalls in step (a) is retained as trench sidewall gate insulation (21A) before depositing gate conductive material (34) in step (f).
- 5. (Currently Amended) A method as claimed in any of claims 1 to 4, The method as recited in claim 1, wherein the doped polysilicon (34) deposited in step (b) is greater than 5e19cm 3. As or P doped polysilicon. is greater than 5 x 10¹⁹ cm⁻³ As-doped or P-doped polysilicon.
- 6. (Currently Amended) A method as claimed in any one of claims 1 to 5, The method as recited in claim 1, wherein in step (d) the doped polysilicon (31) is thermally oxidised at a temperature in the range 650-850°C.
- 7. (Currently Amended) A method as claimed in claim 6, The method as recited in claim 6, wherein the oxidation temperature range is 700-800°C.
- 8. (Currently Amended) A trench-gate silicon semiconductor device (4) manufactured by the method as elaimed in any one of the claims 1-to 7. as recited in claim 1.
- 9. (Currently Amended) A device as claimed in claim 8, The device as recited in claim 8, wherein the device is a vertical power transistor.

10. (Currently Amended) A device as claimed in claim 9, The device as recited in claim 9, wherein the transistor cells have a cell pitch less than 2 micron.

13. (Cancelled)